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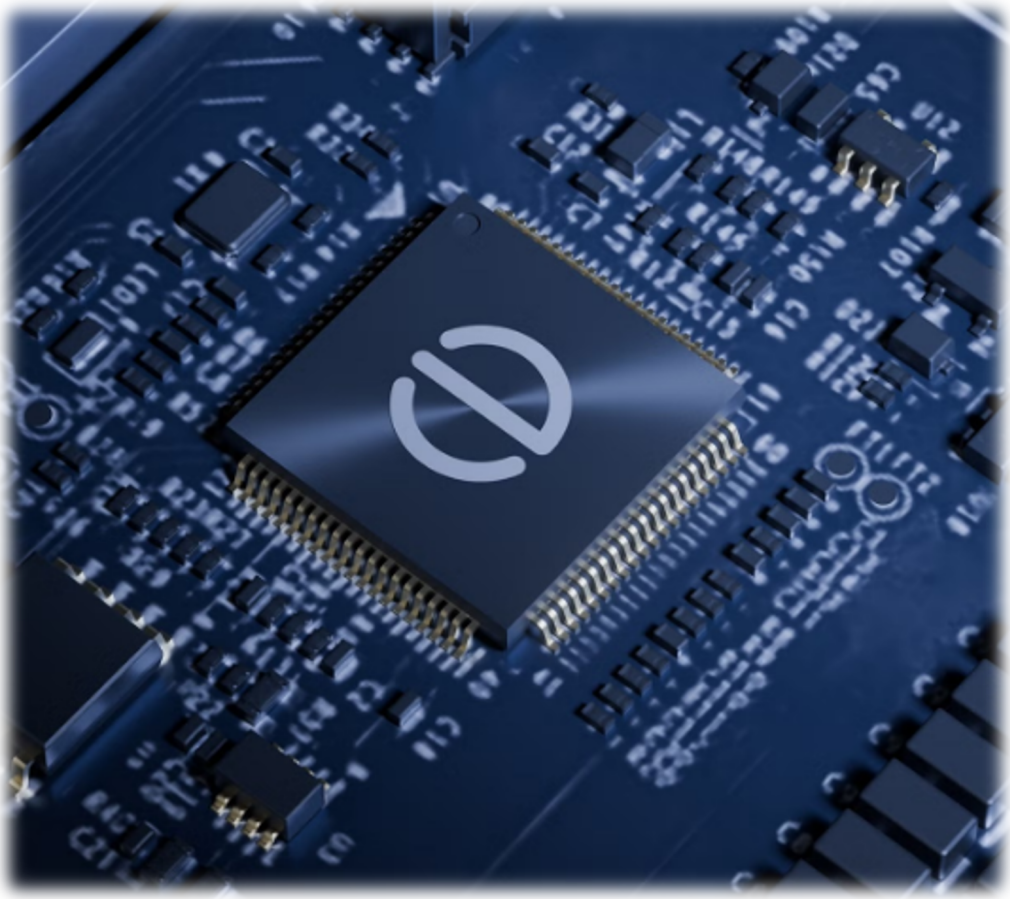
KESTREL ASIC TECHNOLOGY

The Enphase Kestrel ASIC: A Purpose-Built Platform for Intelligent Power Conversion



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A B S T R A C T

The Enphase Kestrel ASIC: A Purpose-Built Platform for Intelligent Power Conversion

The Kestrel application-specific integrated circuit (ASIC) is an Enphase internally developed custom chip and the fifth generation of Enphase's proprietary power conversion silicon. This ASIC is at the heart of Enphase's single-stage power converter technology, enabling high-performance, cost-effective products that would be difficult to realize with off-the-shelf components at comparable levels of performance, reliability, and integration. These products include solar microinverters, battery storage systems, bidirectional chargers, and solid-state transformers (SSTs) designed for medium-voltage grid interfaces in AI data center and other applications.

Fabricated using a mature and cost-effective 22 nm complementary metal-oxide-semiconductor (CMOS) process, the Kestrel ASIC integrates a quad-core ARM Cortex-M4F multi-processor architecture, Enphase's proprietary high-speed power control and analog-to-digital converter (ADC) intellectual property (IP), a custom power line communication (PLC) subsystem, and a comprehensive security and functional safety framework. Reusing the same custom chip across a broad product portfolio establishes a platform intended to support more predictable and shorter product development cycles while maintaining Enphase's hallmark field reliability.

01 Background

The Evolution of Enphase Custom Silicon

Enphase Energy has relied on proprietary custom silicon since the founding of the company. The unique single-stage power converter topology at the heart of every Enphase microinverter depends on precise, high-frequency digital control that is difficult to achieve with off-the-shelf components at comparable cost, performance, and reliability. From the very first Enphase microinverter, engineers recognized that a purpose-built ASIC would be essential to realizing the performance, cost, and reliability goals of the Enphase platform. Where conventional power electronics products can be built around standard pulse-width modulation (PWM) controllers and discrete analog circuitry, Enphase's resonant cycloconverter topology demands real-time algorithms too fast and too tightly coupled to the converter's resonant state to be executed by any general-purpose microcontroller or programmable logic available at competitive cost.

The first four generations of Enphase custom silicon evolved in parallel with the Enphase microinverter product line, growing in capability with each successive product family. Early devices focused primarily on the power conversion control loop, while subsequent generations added power line communication capability — enabling the Enphase microinverter network that allows each module to be individually monitored and managed — and increasingly sophisticated grid-support functions.

A pivotal architectural transition came in 2011, when Enphase engineering leadership recognized that the company's existing dual-interleaved flyback topology would be fundamentally incompatible with an emerging wave of regulatory requirements for smart grid support. The California Public Utilities Commission (CPUC) was revising "Rule 21" — the landmark 1982 framework governing distributed generation — to mandate that grid-connected inverters provide active power factor control and advanced grid functions (AGFs) by 2015 [1]. Domestic and international utilities were drafting similar compliance mandates. Meeting these requirements demanded a new converter topology, and with it, a new ASIC.

Enphase engineers selected a single-stage, dual-active-bridge, series-resonant cycloconverter as the replacement architecture. This topology offered a path to full AGF compliance while enabling superior efficiency and reduced passive component count. Crucially, it also demanded a fundamentally new control algorithm — one that processes high-frequency resonant waveform data and generates gate drive signals with nanosecond accuracy. The new ASIC required custom analog front-end circuits tightly integrated with the digital control engine, running at switching frequencies far beyond the capability of standard PWM-based controllers.

Successive ASIC generations refined this architecture, expanding ADC resolution and sample rates, deepening the PLC communication stack, and adding security features as the growing

Enphase installed base became increasingly important distributed energy infrastructure. By the fourth generation, the Enphase ASIC had grown from a focused power conversion controller into a multi-function system-on-chip supporting an ecosystem of grid-edge applications. With more than 87 million microinverters cumulatively shipped and deployments representing approximately 31.52 GW of cumulative shipped capacity, Enphase's proprietary silicon has been proven across an extraordinarily broad range of field conditions [2].

The Kestrel Generation

The fifth generation, codenamed Kestrel, represents a fundamental step change in integration and capability. Fabricated on a mature 22 nm CMOS process node, Kestrel incorporates a quad-core ARM Cortex-M4F multi-processor architecture, hardware-enforced security isolation across all bus masters, a comprehensive cryptographic subsystem including AES, SHA, TRNG, and public key infrastructure (PKI) support, end-to-end single-bit error correction, double-bit error detection (SECDED) error-correcting bus infrastructure, and a purpose-built tandem function developed specifically for solid-state transformer applications. Kestrel also incorporates Enphase's latest-generation high-speed ADC and power line communication IP.

The result is a highly versatile platform designed to support multiple Enphase product families, including the Enphase IQ Solid-State Transformer (IQ SST) for medium-voltage data center applications, next-generation Enphase IQ Battery storage systems, and the IQ Bidirectional EV Charger [3]. Across all these applications, Kestrel enables the performance, security, and reliability that Enphase products demand, while the breadth of the platform justifies the development investment through reuse across a broad product portfolio.

This white paper provides an in-depth technical description of the Kestrel ASIC: its multi-processor architecture, protection and security model, functional safety design, key custom IP blocks, and its enabling role in the Enphase IQ SST power module.

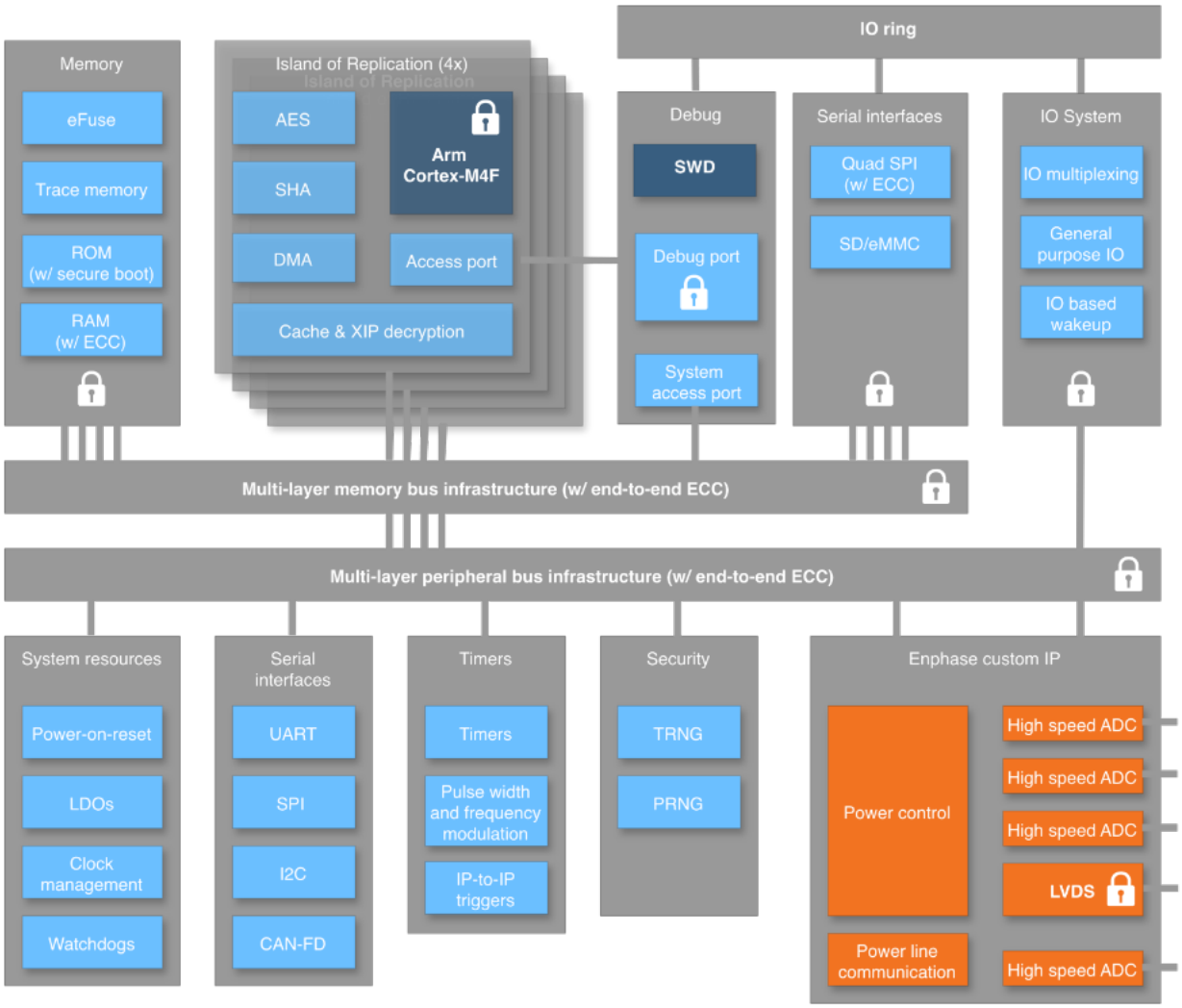
02 Architecture Overview

The Kestrel ASIC is specifically engineered for high-efficiency, single-stage power conversion. It is housed in a thermally enhanced eLQFP package. This packaging features exposed gull-wing leads designed to improve mechanical stress resistance, an important consideration for products designed for long field life, including Enphase solar microinverters.

To ensure manufacturing quality and field reliability, the ASIC incorporates:

- Robust design for test (DfT): High stuck-at and at-speed test coverage facilitates the early detection of manufacturing defects, ensuring only high-integrity devices reach the final product assembly.

- Operational longevity: The architecture is designed with significant performance margins to accommodate component derating, maximizing long-term reliability in demanding environments.



Enphase Energy Kestrel ASIC architecture

The ASIC utilizes a multi-processor architecture featuring four identical islands of replication (IoR). Each IoR is equipped with an ARM Cortex-M4F processor, a dedicated DMA controller, and integrated cryptography accelerators.

By employing a defined software convention, each island is assigned a distinct, isolated role. In a microinverter product, the functional distribution is structured as follows:

- Island 0, Secure Boot: Manages hardware-rooted trust and cryptographic integrity. This island effectively implements a secure enclave within the chip.

- Island 1, Power Conversion: Dedicated to the high-speed execution of power control algorithms.
- Island 2, PLC: Governs the dedicated communication stack.
- Island 3, Application Services: Executes the primary system application via a real-time operating system (RTOS).

This architectural separation significantly streamlines product development by allowing each core function to be developed, validated, and optimized in isolation, reducing cross-functional complexity and enhancing system stability.

To optimize performance, each IoR features a read-only cache designed to minimize latency for code execution from external memory, such as NOR Flash interfaced via the Quad SPI controller. For internal memory operations (ROM and RAM), the cache is bypassed, as these memories natively support zero-wait-state (0 bus cycle) latency.

The chip memory bus infrastructure is multi-layered and shared memory resources are multi-ported. These multi-ported memories are arbitrated with a bandwidth guarantee. The peripheral bus infrastructure consists of different bus groups. Each bus group is associated with one or multiple islands. This association is enforced through protection units in the peripheral bus infrastructure. The lock symbols in the block diagram illustrate the presence of protection functionality in the chip. The multi-layered bus infrastructures, memory arbitration, and association of peripheral groups to specific islands all contribute to predictable execution behavior, a desirable quality for embedded systems.

The chip leverages a strategic mix of industry-standard and proprietary IP to balance ecosystem compatibility with technical differentiation. Standard IP — including ARM processors and common interfaces like I2C, UART, SPI, and CAN-FD — allows for seamless integration with established tools. Meanwhile, custom IP, specifically high-speed ADCs, power controllers, low voltage differential signaling (LVDS) controller, and power line communication, provides superior performance and cost-efficiency for power conversion products. This high level of integration creates a versatile platform, justifying development costs through reuse across a broad product portfolio.

Debugging is provided by a standard ARM serial wire debug (SWD) interface. This interface is connected to a debug port (DP), which is connected to five separate access ports (APs): one dedicated to each of the four IoR processors for individual debugging, and a fifth system AP that provides direct, transparent access to the entire chip bus infrastructure. This setup ensures comprehensive monitoring and diagnostic capabilities across the entire ASIC.

03 Protection

The Kestrel ASIC implements a multi-layered protection architecture designed to ensure both security and functional safety. While the integrated ARM Cortex-M4F utilizes a standard memory protection unit (MPU) to isolate individual software tasks, this single-processor mechanism is insufficient for multi-processor environments [4].

To address this, the ASIC incorporates custom chip-level protection units (represented by the lock symbols in the block diagram) that regulate access for all bus masters, whether internal — such as processors, DMA controllers, and cryptography accelerators — or external, via ARM SWD and LVDS interfaces.

Key features of this protection scheme include:

- Identity-based access: Every bus transfer is tagged with a unique bus master identifier, allowing protection units to enforce restrictions based on this identifier, target address, and access attributes.
- Granular isolation: The protection units can restrict specific memories or peripherals to dedicated masters or facilitate secure sharing for inter-processor communication.
- Per IO cell protection: Each IO cell in the IO ring features a dedicated protection unit, enabling the complete isolation of processors or functional "islands."

By combining ARM MPUs for task isolation with custom chip-level units for bus master isolation, the ASIC prevents malicious access to confidential data and ensures that software errors in one processor cannot interfere with the operation of another.

To enable seamless data exchange between processors, the chip-level protection units support shared memory apertures. Specific RAM ranges can be designated as shared buffers. Within the protection units, these ranges are mapped to multiple bus masters simultaneously. Similarly, the protection units can be programmed to allow multiple bus masters to access a single peripheral (like an inter-processor communication IP) to coordinate synchronization signals.

04 Security and Cryptography

The Kestrel ASIC implements a multi-layered security architecture that combines hardware protection with cryptographic services. While hardware protection units restrict unauthorized access, the cryptographic services ensure data confidentiality, integrity, authentication, and non-repudiation.

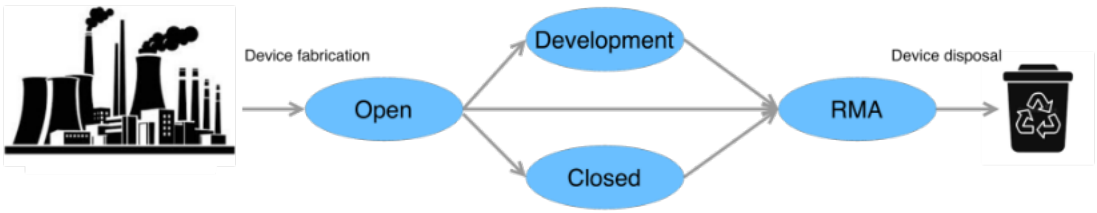
To support these security objectives, the ASIC utilizes dedicated hardware cryptography accelerators and optimized software:

- Cipher and hashing hardware: Each IoR contains dedicated AES [5] and SHA IPs [6]. These function as bus masters with unique identifiers, allowing the ASIC's protection units to enforce granular, restricted access to sensitive data. The AES IP supports multiple modes, notably AES-GCM for simultaneous encryption, integrity, and authentication, while the SHA IP facilitates certificate signature calculations.
- Asymmetric cryptography: Public key operations are implemented in software. To defend against timing-based side-channel attacks, these implementations utilize constant-execution-time algorithms. Combined with hardware acceleration, this supports a complete, certificate-based PKI.
- Entropy and key management: A custom true random number generator (TRNG) IP leverages unpredictable physical device properties to generate high-entropy values for key generation, authentication challenges, and seeding of a custom pseudo random number generator (PRNG) IP.
- Secure storage: Long-term secrets, device-unique identifiers, and trim information are stored in internal eFuse memory. Access to this non-volatile storage is strictly governed by chip-level protection units to prevent unauthorized exposure.

The TRNG IP facilitates the introduction of stochastic delays into the bus transfers of IoR bus masters. This feature can be enabled independently for each IoR, creating non-deterministic execution timing. By injecting this unpredictability, the architecture effectively mitigates the risk of timing-based side-channel attacks, significantly enhancing the chip's overall security posture.

05 Lifecycle Management

The Kestrel ASIC implements a structured lifecycle management architecture, where each lifecycle stage defines the operational state and security posture of the device from initial fabrication to end-of-life. These stages are managed via internal eFuse storage and governed by secure ROM boot code functions to ensure only authorized transitions.



Authorized lifecycle stage transitions

The device supports the following four lifecycle stages:

- Open: This is the default state for newly fabricated devices. The eFuse is programmed with essential trim and calibration data and contains limited, non-unique security information. At this stage, the SWD port is disabled for processor access, and automated test equipment (ATE) is restricted to limited device interaction.
- Development: Designated for firmware engineering and system integration, this stage contains device-unique security information within the eFuse. The SWD port is fully enabled, providing the processor access necessary for debugging and development.
- Closed: The production-ready state for devices integrated into final products. This stage contains device-unique security information within the eFuse, but access is restricted. The SWD port is fully disabled, and ATE access is limited to facilitate a transition to the RMA (return material authorization) stage if required.
- RMA: Utilized for failure analysis of field-returned devices. To protect intellectual property and sensitive data, all eFuse security information is permanently erased. In this state, ATE is granted comprehensive device access to perform exhaustive diagnostics and analysis.

06 Secure Boot Architecture

Following a power-on-reset (PoR), the chip establishes a secure, isolated execution environment. This architecture is anchored by a hardware-immutable root of trust (RoT) residing in ROM, alongside unique device identifiers and confidential data protected within eFuse storage.

First Stage Boot (ROM)

At initialization, island 0 assumes exclusive responsibility for the secure boot sequence. The island 0 processor begins executing directly from its ROM reset vector while all other islands (1, 2, and 3) are kept in a reset state. Because of its immutable nature, the ROM boot code is restricted to essential primitives, acting as the first stage of a multi-stage boot process.

Depending on the current device lifecycle stage in eFuse memory, the ROM boot code executes the following foundational security and initialization functions:

- Integrity verification: Performs ROM integrity checks and mandatory cryptographic self-tests.
- Hardware initialization: Invalidates the island 0 cache, initializes internal RAM, and starts the DMA controller "scrubber" mode.

- Peripherals and interfaces: Deploys trim, calibration, and hardware protection unit profiles; enables the Quad SPI controller, cryptography IP, TRNG IP, and the SWD interface.
- Countermeasures and monitoring: Activates non-deterministic execution timing to mitigate side-channel attacks and enables hardware watchdog timers (WDTs).

Chain of Trust Progression

To extend the chain of trust, the ROM code validates the integrity and authenticity of the second-stage boot image located in external Flash memory. Once authenticated, the second-stage image is decrypted into internal RAM based on a device-unique identifier stored in eFuse storage. This device-unique identifier is only accessible by the first-stage boot.

Control is then transferred to the second stage. Because subsequent boot stages reside in Flash memory, they support secure over-the-air (OTA) updates, providing operational flexibility. Ultimately, a downstream boot stage authenticates the firmware for islands 1, 2, and 3, releasing those processors from reset to initiate standard system operations. This authentication is based on PKI certificates. In addition, a PKI certificate is used for chip identification.

07 Functional Safety

The Kestrel ASIC implements a functional safety architecture designed to mitigate unintended hardware and software failures, distinguishing these efforts from security measures aimed at malicious intent. The architecture leverages a combination of hardware-level protection, data redundancy, and temporal monitoring to ensure continuous, reliable operation.

To prevent cross-domain interference, hardware protection units enforce strict isolation. These units restrict address space access, ensuring that unintended operations from one bus master cannot compromise another bus master's protected address space.

The ASIC utilizes SECDED to safeguard data across two primary states:

- Data in Storage: SECDED protects internal caches, RAM, and external NOR Flash (interfaced via the Quad SPI controller) against soft errors such as cosmic ray bit-flips and hard physical cell failures. IoR DMA controllers feature a dedicated "scrubber" mode that periodically verifies parity and corrects single-bit errors. This proactive measure prevents the accumulation of single-bit errors into uncorrectable double-bit errors. Scrubbing operations are assigned low bus arbitration priority to minimize impact on dynamic system performance.

- Data in Motion: All bus transfers utilize an end-to-end error correcting code (ECC). Bus masters append SECDED parity to each transfer, which the bus targets verify and correct in real-time.

To complement data-level protections, the ASIC deploys multiple WDTs driven by independent clock sources. While SECDED maintains data accuracy, the WDT subsystem ensures temporal integrity by detecting software stalls and hardware hangs, guaranteeing deterministic forward progress.

All detected errors — single-bit errors, double-bit errors, WDT expirations — are logged and reported via a centralized fault infrastructure. This diagnostic data serves a dual purpose: providing immediate chip-level alerts and corrective actions and enabling long-term predictive maintenance scheduling to replace degrading products before a critical failure occurs.

08 Power Controller

The power controller is the most critical custom IP block on the Kestrel ASIC, and the primary reason Enphase designs its own silicon. Conventional off-the-shelf microcontrollers and programmable logic devices are not well suited to execute the control algorithms that Enphase's single-stage, dual-active-bridge, series-resonant cycloconverter demands at the switching frequencies and latencies required. The power controller is a purpose-built hardware digital controller: a fully deterministic signal processing pipeline running directly at the converter switching frequency, with hard-wired interfaces to the high-speed ADC outputs and the gate driver command registers in the IO ring.

The Resonant Converter Control Problem

The single-stage resonant cycloconverter at the heart of every Enphase microinverter and IQ SST power module operates by switching a network of Gallium Nitride (GaN) bidirectional switch (BDS) devices to drive current through a high-frequency transformer and a series resonant tank — a tuned LC circuit that transfers energy efficiently across the galvanic isolation boundary [7]. The switches fire at a rate of hundreds of kilohertz, many orders of magnitude above the 50/60 Hz utility grid frequency, creating a synthetic high-frequency waveform that is transformed and then shaped to produce the desired output. Enphase's single-stage topology performs both the high-frequency conversion and the grid-frequency synthesis in a single power stage, in contrast to the two- or three-stage designs used by conventional grid-connected inverters.

Controlling this topology requires real-time, cycle-by-cycle knowledge of the resonant tank state — the instantaneous combination of capacitor voltage and inductor current that defines the converter's operating point at any moment. From this state, the controller must determine the precise timing of every gate transition across the GaN switch bridges to maintain the desired

energy transfer while simultaneously regulating the output and maintaining grid compliance. This computation must complete within a small fraction of the switching period — a window measured in nanoseconds to low microseconds — leaving little practical margin for the latency associated with firmware-based execution paths.

Hardware Control vs. Software PWM

Conventional power electronics controllers pair a microcontroller or DSP with a PWM timer peripheral. The processor runs a control algorithm in firmware: it reads ADC samples, computes a duty cycle or phase shift, and writes the result into a compare register. This software-in-the-loop architecture has an unavoidable latency floor set by the execution time of the firmware control path — typically several microseconds or more, even on fast processors with hardware floating-point units. For slowly switching converters this is acceptable. For Enphase's resonant cycloconverter, where a complete switching cycle spans only a few microseconds, firmware latency would consume an unacceptably large fraction of the available control window.

The Kestrel power controller eliminates this bottleneck entirely. The complete control sequence — from ADC sample acquisition through state estimation, trajectory computation, and gate command generation — is implemented in custom digital hardware and executes in a fixed, deterministic number of clock cycles. There is no firmware in the control path: the hardware pipeline runs autonomously, clocked at the ASIC system frequency, and delivers gate commands with nanosecond-scale latency from the moment the ADC samples are available. The result is a closed-loop control bandwidth exceeding 100 kHz — an order of magnitude or more beyond what firmware-based implementations can achieve at comparable switching frequencies.

Trajectory-Based Control

Rather than computing a simple duty cycle or phase-shift value, the Kestrel power controller implements a trajectory-based control algorithm. The controller continuously tracks the instantaneous state of the resonant tank and, from this state, computes the optimal sequence of gate transitions — the switching trajectory — that will steer the converter toward the desired operating point along the most efficient path consistent with the tank's natural resonant dynamics.

This approach has three important consequences. First, it is inherently predictive: the algorithm uses knowledge of the resonant tank's physics to schedule future gate events rather than reacting to errors after the fact, enabling tighter regulation with less overshoot. Second, it naturally implements soft switching across the full operating range. Because gate transitions are timed to coincide with the natural zero-crossing of switch voltage and current, switching losses are minimized without requiring a separate soft-switching control mode — a significant efficiency and reliability benefit that holds from zero load to full power. Third, the algorithm is inherently large-signal stable: because it tracks the physical state of the converter directly rather than operating on a linearized small-signal model, it maintains high performance across the full input voltage and load range without gain scheduling or operating-point-dependent tuning.

Control Bandwidth and System Response

The power controller's closed-loop bandwidth of more than 100 kHz translates directly into the IQ SST's headline system advantage: sub-millisecond transient response to sudden load changes. Conventional SST designs using high-voltage Silicon Carbide (SiC) switches operate at much lower switching frequencies, which limits control bandwidth and means they require multiple AC line cycles — tens of milliseconds — to respond to a load step. In contrast, the Enphase IQ SST responds in less than 1 ms, approximately one thousand times faster, enabling it to ride through the dynamic load profiles characteristic of AI data center GPU racks, which can swing between 10% and 100% of rated power multiple times per second.

This speed advantage is qualitative as well as quantitative. A system that responds within one millisecond can track load changes as they occur, potentially eliminating the need for local supercapacitor energy buffers that would otherwise be required to bridge the gap between a load step and the converter's response. That same speed advantage also enables transferring loads between different feeds in the event of outages or faults, potentially eliminating the need for local battery energy buffers such as uninterruptible power supplies (UPS) or battery backup units (BBU). Both these energy buffering functions can be performed by large-scale battery energy storage systems located remotely — outside the data center, where safety, space, and cost constraints are far less severe.

Three-Phase Support

A further differentiating capability of the Kestrel power controller is its native support for three-phase power conversion. In addition to the single-phase AC bridge used in residential microinverter applications, the hardware control engine directly supports three-phase and three-phase-plus-neutral AC bridge configurations. In the three-phase configuration, the controller simultaneously manages gate transitions across three switch legs, maintaining coherent 120-degree or 180-degree phase relationships using an algorithm that is fully sequence component aware. The three-phase-plus-neutral configuration adds a fourth leg to handle the neutral conductor, accommodating asymmetric loads and single-phase branch circuits within the same three-phase system. Because the hardware pipeline computes all gate events in a small number of clock cycles irrespective of the number of active legs, the three-phase control loop operates at the same sub-microsecond latency as the single-phase case. This native three-phase capability is a key enabler for the Enphase IQ Battery to support split-phase and three-phase AC configurations.

09 High-Speed ADCs

The four 100 Msps high-speed ADCs on the Kestrel ASIC are the primary measurement interface for the power controller described in the preceding section. Designed for high-frequency signal precision, the converters sample resonant tank current waveforms at sufficient rate to fully resolve the instantaneous converter state. One of the ADCs incorporates an integrated analog front end (AFE) with a multiplexer to enable sequential multi-signal measurement. These converters serve dual roles in power line communications and power control.

For power control, the ADC requirements are especially demanding. Enphase's resonant tank topology relies on accurate measurement of high-frequency signals at a high sample rate, and measurements must incur minimal latency to allow for tight hardware-based power control. The combination of 100 Msps sample rates and the direct hardware integration between the ADC output and the power control IP enables the sub-microsecond control loop execution times that differentiate Enphase's resonant converter products from conventional PWM-based alternatives.

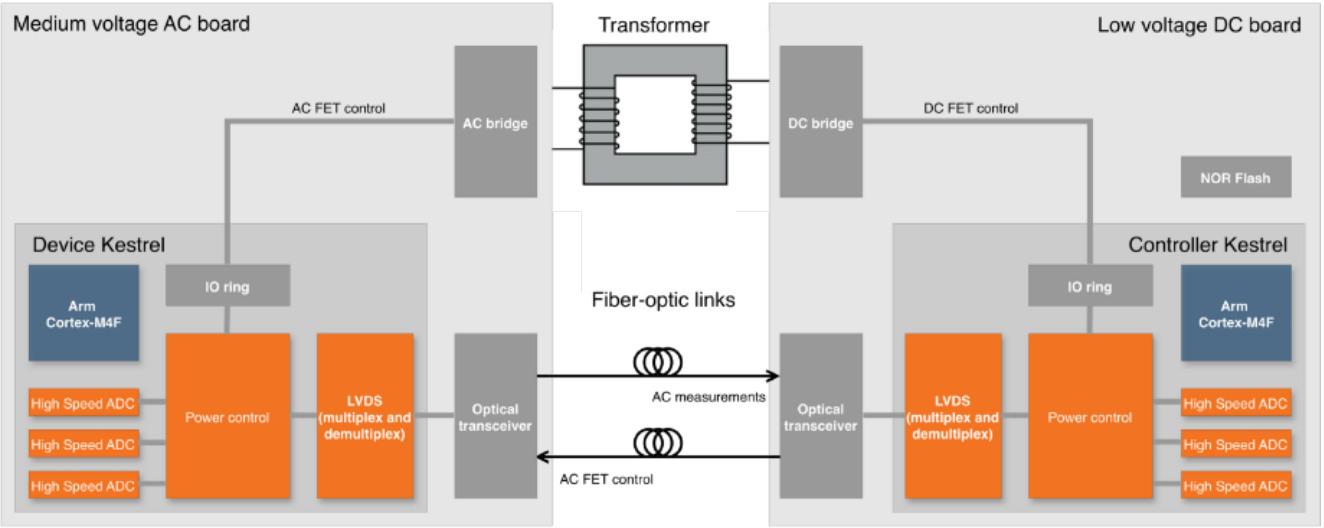
10 Enphase IQ SST Technology

The Enphase IQ SST power module will convert power between a medium-voltage AC distribution network and a low-voltage DC bus, replacing the conventional line-frequency transformer with an all-electronic solid-state design. The module will bring together the tandem Kestrel control architecture and the single-stage resonant power conversion technology described in the preceding sections. Beyond the headline performance advantages of that combination — sub-millisecond transient response and native three-phase capability — the high-frequency soft-switching operation yields additional system-level benefits:

- Reduced switching losses and passive component count relative to conventional hard-switched topologies.
- Low electromagnetic interference (EMI) signature, which permits a cost-effective plastic enclosure rather than the metallic shielding required by hard-switched alternatives.

The module uses separate medium-voltage and low-voltage boards across an isolation boundary. A critical design challenge is this isolation boundary between these two boards. The power module will use transformer (magnetic) isolation for power transfer and optical isolation for power control information.

The IQ SST power module will use a tandem configuration of two Kestrel chips. In this configuration, the two Kestrel chips will provide distributed, coordinated power control. The power control IP exchanges power control information over two uni-directional fiber-optic links.



IQ SST power module — tandem configuration of two Kestrel chips

Within the tandem configuration, the low-voltage domain Kestrel chip will take the lead in the power conversion. This chip is identified as the “Controller Kestrel,” whereas the other chip is identified as the “Device Kestrel.” The Device Kestrel conveys AC power domain measurements to the Controller Kestrel. The Controller Kestrel conveys AC FET control to the Device Kestrel.

LVDS Controller

The fiber-optic isolation link between the two Kestrel ASICs in the IQ SST power module is driven by the Kestrel's custom LVDS controller IP. This LVDS controller interfaces with an external optical transceiver chip and serializes and deserializes multiple logical power-control streams into a single LVDS bitstream as illustrated below.

Controller to Device Kestrel	Device to Controller Kestrel
AC FET control information	AC power domain measurements
Remote shutdown request	Remote shutdown request
Remote chip access	Remote chip access

Logical power-control streams multiplexed into LVDS bitstream

The remote chip access enables the Controller Kestrel to access the 32-bit address space of the Device Kestrel and vice versa. The LVDS controller includes a hardware protection unit to restrict these accesses. The Controller Kestrel uses remote access to upload code in the Device Kestrel internal RAM, eliminating the need for an external NOR Flash chip on the medium-voltage board.

The external optical transceiver chip requires the LVDS bitstream to be DC balanced. The LVDS controller accomplishes this through scrambling and 6b/8b coding. Latency-critical streams are scrambled to minimize transmission delays. Latency-tolerant streams use 6b/8b coding, which ensures DC balance and provides built-in error detection capabilities.

11 Power Line Communication

Kestrel-based products for PV applications usually communicate over the power line itself — the AC wiring that connects each device to the grid. The Kestrel ASIC features a custom PLC IP, enabling high-reliability, in-band data transmission over existing electrical infrastructure without requiring a separate communication wiring run.

The PLC operates within the 95–125 kHz band, which is unregulated according to CENELEC (European) [8] and FCC (American) [9] standards. CENELEC specifically designates this band for high-reliability, in-premise use. Within the band, the PLC software stack dynamically balances effective bitrate against baud rate, modulation complexity, and error correction. In adverse operating conditions, the system automatically shifts to simpler modulation or enhanced error correction to prioritize connection stability over raw speed.

For noise mitigation, the PLC deploys:

- A high-performance bandpass filter.
- Forward error correction (FEC).
- Bit interleaving: Combined with FEC to mitigate impulse noise caused by events synchronous to the AC line frequency or high-power device switching events.

Within a solar microinverter product, the PLC IP enables the following critical functions between microinverters and on-site gateways:

- OTA updates: Enables remote firmware enhancements without physical intervention.
- Telemetry and monitoring: Transmits real-time solar panel status and diagnostic data.
- Predictive maintenance: Data forwarded to the cloud supports comprehensive reporting and allows for proactive system servicing based on diagnostic trends.

12 Conclusion

The Kestrel ASIC builds on two decades of Enphase investment in proprietary power conversion silicon and extends that foundation into a broader platform for intelligent energy products. The decision to develop a purpose-built ASIC — rather than rely on commodity microcontrollers or configurable logic — reflects a core conviction that the performance, cost, reliability, and differentiation required to compete at the frontier of distributed power electronics must be designed in, not assembled from generic components. Kestrel validates that conviction across every dimension of its architecture.

A Platform, Not a Product

The most important attribute of the Kestrel ASIC is not any single technical feature but the breadth of applications it enables from a single silicon platform. Solar microinverters, battery storage systems, bidirectional EV chargers, and now solid-state transformers for medium-voltage data center power distribution all share the same control ASIC. This platform reuse compresses product development timelines and allows Enphase to amortize the substantial cost of 22 nm CMOS development across a diverse and growing product portfolio.

Security and Safety by Design

The depth of Kestrel's security architecture — hardware-rooted trust, cryptographic acceleration across all four processor islands, identity-based bus access control, lifecycle management from fabrication to end-of-life, and non-deterministic execution timing for side-channel protection — reflects Enphase's recognition that its large deployed base of grid-connected microinverters forms part of increasingly important distributed energy infrastructure. As grid-connected power electronics play an ever-larger role in energy systems, the security posture of every device on the distribution network matters. Kestrel was designed with this responsibility in mind.

Equally, the functional safety architecture — SECDED protection across all data paths, DMA scrubbing, multiple independent watchdog timers, and a centralized fault infrastructure — ensures that Kestrel-based products can meet the reliability demands of a 25-year solar microinverter warranty and the high availability expectations of data center-grade SST applications.

Enabling the IQ SST

The Kestrel tandem function is perhaps the most novel capability introduced in this generation. The ability for two Kestrel ASICs — separated by the tens of thousands of volts of medium-voltage isolation — to operate as a coordinated, single-controller pair via a fiber-optic link is not a feature that could have been added to an existing off-the-shelf microcontroller. It required hardware IP specifically designed for this purpose, integrated into the ASIC at the silicon level. This capability enables the IQ SST power module to inherit Enphase's complete microinverter control stack,

including years of proven field reliability, while crossing the medium-voltage isolation boundary cleanly and with reduced component complexity.

The Path Forward

Kestrel is a platform designed for longevity. Its architecture includes significant performance margins against component derating, a formal lifecycle management scheme that supports the full product lifespan from development through field deployment and end-of-life, and a security model that can be updated via secure OTA firmware without requiring hardware changes. As the Enphase product portfolio continues to expand — and as the demands of grid-edge power electronics grow with the energy transition — Kestrel is expected to provide a foundation that can evolve with these requirements while supporting Enphase's continued differentiation in distributed power electronics.

13 References

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